UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/684,529	10/06/2000	John D. Logue	X-735 US	1502

24309 7590 08/08/2005

XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
ZHENG, EVA Y	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/684,529	LOGUE ET AL.	
	Examiner	Art Unit	
	Eva Yi Zheng	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,12,13 and 18-22* is/are rejected.

7)☒ Claim(s) *4-11 and 15-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection due to amendment.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 3, 12, 13, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Lundberg et al. (US 5,511,100).

a) Regarding claim 1, Lundberg et al. disclose a digital clock manager having a reference input terminal (reference clock in Fig. 1), a skew input terminal (output of block 16 in Fig.1), an output terminal ("behind and ahead" in Fig. 1), and a frequency adjusted output terminal ("slow, fast" in Fig. 1), the digital clock manager comprising (as shown in Fig. 1):

a delay lock loop (DLL) (inherent as block 12 in Fig. 1) coupled to the reference input terminal (reference clock in Fig. 1), the skew input terminal (output of block 16 in Fig.1), and the output terminal ("behind and ahead" in Fig. 1), wherein the delay lock loop generates an output clock signal at the output terminal (Col 5, L1-3); and

a digital frequency synthesizer (11 in Fig. 1), having a variable oscillator (inherent as block 16 in Fig. 1), coupled to the delay lock loop (as shown) and the frequency adjusted output terminal, wherein the digital frequency synthesizer generates a frequency adjusted clock signal at the frequency adjusted output terminal ("slow, fast" in Fig. 1).

b) Regarding claim 2, Lundberg et al. disclose the digital clock manager of Claim 1, wherein the delay lock loop (block 12 in Fig. 1) synchronizes a reference clock signal (reference clock in Fig. 1) on the reference input terminal with a skewed clock signal on the skew input terminal (inherent as block 16 in Fig. 1) (Col 4, L61- Col 5, L 3).

c) Regarding claim 3, Lundberg et al. disclose the digital clock manager of Claim 1, wherein the frequency adjusted clock signal is synchronized with the output clock signal during concurrences (Col 4, L2-20).

d) Regarding claim 12, Lundberg et al. disclose the digital clock manager of Claim 1, further comprising a variable delay circuit coupled between the delay lock loop and the output terminal (block 16 in Fig.1).

e) Regarding claim 13, Lundberg et al. disclose the digital clock manager of Claim 1, further comprising a variable delay circuit coupled between the digital frequency synthesizer and the frequency adjusted output terminal (block 16 in Fig.1).

f) Regarding claim 18, Lundberg et al. disclose the digital clock manager of Claim 1, wherein the digital frequency synthesizer performs a frequency search while the delay lock loop is performing lock acquisition (block 11 and 12 as shown in Fig. 1).

4. Claims 19-22 are rejected under 35 U.S.C. 102(a) as being anticipated by Waizman (IEEE Feb. 1994).

a) Regarding claim 19, Waizman discloses a method to generate an output clock signal and a frequency adjusted clock signal from a reference signal (CLK in Fig. 2), wherein the output clock signal (V_{CNTL} in Fig. 2) is synchronized with the frequency adjusted clock signal (CLK in Fig. 2) during a concurrence; the method comprising:

generating a synchronizing clock signal (Col 1, L30-32);

matching a DLL output delay with a DFS output delay (as shown in Fig. 3);

generating the output clock signal lagging the synchronizing clock signal by the DLL output delay (T_D in Fig. 3 and paragraph 4 by Waizman); and

generating the frequency adjusted clock signal so that an active edge of the frequency adjusted clock signal lags an active edge of the synchronizing clock signal by the DFS output delay during the concurrence (as shown in Fig. 3 and 4).

b) Regarding claim 20, Waizman discloses the method of Claim 19, wherein the step of matching a DLL output delay with a DFS output delay comprises synchronizing a DLL output circuit with a DFS output circuit (as shown in Fig. 2).

c) Regarding claim 21, Waizman discloses the method of Claim 19, further comprising performing lock acquisition (CONTROL in Fig. 3).

d) Regarding claim 22, Waizman discloses method of Claim 21, further comprising the performing a frequency search during lock acquisition (CONTROL in Fig. 3).

Allowable Subject Matter

5. Claims 4-11 and 15-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eva Y Zheng whose telephone number is 571 272-3049. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eva Yi Zheng
Examiner
Art Unit 2634

July 25, 2005

SHUWANG LIU
PRIMARY EXAMINER